CLAIMS

What is claimed is:

1. A method comprising:

mapping a plurality of exception masks in a source architecture to an exception mask in a target architecture;

executing translated code in the target architecture, the translated code representing binary code in the source architecture; and

determining a state for the source architecture if an exception is raised while executing the translated code.

2. The method of claim 1, wherein determining a state comprises:

determining an excepted instruction in the source architecture corresponding to the translated code that raised the exception;

restoring the state of the source architecture to a pre-instruction state;

masking all exceptions in the exception mask in the target architecture;

re-executing the translated code corresponding to the excepted instruction; and

analyzing a result of re-executing the translated code.

3. The method of claim 2, wherein analyzing a result comprises:

determining an exception type for the exception that was raised; and

examining the exception mask in the source architecture associated with the excepted instruction.

4. The method of claim 1 further comprising:

selecting the state for the source architecture based on an exception type if the exception is genuine.

5. The method of claim 1 further comprising:

selecting a post-instruction state for the source architecture if the exception is erroneous.

6. The method of claim 1, wherein mapping a plurality of exception masks comprises:

performing a logical AND operation on the plurality of exception masks.

7. The method of claim 1 further comprising:

determining a translated code block to use as the translated code based on the exception mask in the target architecture.

8. The method of claim 7 further comprising:

checking the exception mask against a masking assumption for the translated code block.

9. The method of claim 8 further comprising:

generating two translated code blocks, an optimized code block with a masking assumption that all exceptions are masked and a conservative code block with a masking assumption that an exception is unmasked.

10. The method of claim 7, wherein determining a translated code block comprises:

recognizing when the exception mask in the target architecture is changed by an instruction in the source architecture.

11. A machine-readable medium providing instructions, which when executed by a processing unit, causes the processing unit to perform operations comprising:

mapping a plurality of exception masks in a source architecture to an exception mask in a target architecture;

executing translated code in the target architecture, the translated code representing binary code in the source architecture; and

determining a state for the source architecture if an exception is raised while executing the translated code.

12. The machine-readable medium of claim 11, wherein determining a state comprises:

determining an excepted instruction in the source architecture corresponding to the translated code that raised the exception;

restoring the state of the source architecture to a pre-instruction state;

masking all exceptions in the exception mask in the target architecture;

re-executing the translated code corresponding to the excepted instruction; and

analyzing a result of re-executing the translated code.

13. The machine-readable medium of claim 12, wherein analyzing a result further comprises:

determining an exception type for the exception that was raised; and

examining the exception mask in the source architecture associated with the excepted instruction.

14. The machine-readable medium of claim 11 further comprising:

selecting the state for the source architecture based on an exception type if the exception is genuine.

15. The machine-readable medium of claim 11 further comprising:

selecting a post-instruction state for the source architecture if the exception is erroneous.

16. The machine-readable medium of claim 11, wherein mapping a plurality of exception masks comprises:

performing a logical AND operation on the plurality of exception masks.

17. The machine-readable medium of claim 11 further comprising:

determining a translated code block to use as the translated code based on the exception mask in the target architecture.

18. The machine-readable medium of claim 17 further comprising:

checking the exception mask against a masking assumption for the translated code block.

19. The machine-readable medium of claim 18 further comprising:

generating two translated code blocks, an optimized code block with a masking assumption that all exceptions are masked and a conservative code block with a masking assumption that an exception is unmasked.

20. The machine-readable medium of claim 17, wherein determining a translated code block comprises:

recognizing when the exception mask in the target architecture is changed by an instruction in the source architecture.

21. An apparatus comprising:

a processing unit coupled to a memory through a bus; and

a binary translation process executed from the memory by the processing unit to cause the processing unit to map a plurality of exception masks in a source architecture to an exception mask associated with the processing unit, execute translated code representing binary code in the source architecture, and determine a state for the source architecture if an exception is raised while executing the translated code.

22. The apparatus of claim 21, wherein the binary translation process further causes the processing unit to determine an excepted instruction in the source architecture corresponding to the translated code that raised the exception, restore the state of the source architecture to a pre-instruction state, mask all exceptions in the exception mask associated with the processing unit, re-execute the translated code corresponding to the excepted instruction, and analyze a result of re-executing the translated code to determine a state for the source architecture.

23. The apparatus of claim 14, wherein the binary translation process further causes the processing unit to determine an exception type for the exception that was raised, and examine the exception mask in the source architecture associated with the excepted instruction to analyze a result.

24. The apparatus of claim 21, wherein the binary translation process further causes the processing unit to select the state for the source architecture based on an exception type if the exception is genuine.

25. The apparatus of claim 21, wherein the binary translation process further causes the processing unit to select a post-instruction state for the source architecture if the exception is erroneous.

26. The apparatus of claim 21, wherein the binary translation process further causes the processing unit to perform a logical AND operation on the plurality of exception masks to map the plurality of exception masks to the exception mask associated with the processing unit.

27. The apparatus of claim 21, wherein the binary translation process further causes the processing unit to determine a translated code block to use as the translated code based on the exception mask in the target architecture.

28. The apparatus of claim 27, wherein the binary translation process further causes the processing unit to check the exception mask against a masking assumption for the translated code block.

29. The apparatus of claim 28, wherein the binary translation process further causes the processing unit to generate two translated code blocks, an optimized code block with a masking assumption that all exceptions are masked and a conservative code block with a masking assumption that an exception is unmasked.

30. The apparatus of claim 27, wherein the binary translation process further causes the processing unit to recognize when the exception mask associated with the processing unit is changed by an instruction in the source architecture to determine the translated code block.